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# Dynamic Response of a-InGaZnO Thin-Film Transistors for Ultra-High Definition Active-Matrix Liquid Crystal Displays

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**Abstract:** *The dynamic response of amorphous In-Ga-Zn-O (a-IGZO) thin-film transistors (TFTs) are compared with hydrogenated amorphous silicon (a-Si:H) TFTs. We study the storage capacitor ( $C_{st}$ ) charging characteristics by applying gate and data voltage waveforms for ultra-high definition (UHD) active-matrix flat-panel displays (AM-FPDs). Experimental data show that the charging characteristics of a-Si:H TFTs is clearly inadequate for UHD AM-FPDs and that a-IGZO TFTs are at least capable of supporting up to 8K×4K resolution at 480 Hz. The impact of the gate voltage falling edge on feedthrough voltage ( $\Delta V_p$ ) is investigated in detail. Although for the same  $C_{st}$  the  $\Delta V_p$  is larger for a-IGZO TFT than a-Si:H TFTs,  $C_{st}$  of the a-IGZO TFT can be made larger to reduce  $\Delta V_p$  without obvious degradations in charging behavior. Gate overdrive operation is also demonstrated for a-IGZO TFTs to improve charging characteristics without visible impact on  $\Delta V_p$ . Our results show that the a-IGZO TFT is a suitable technology for next-generation UHD high-frame rate AM-FPDs.*

**Keywords:** AM-FPD; active-matrix; flat-panel displays; thin-film transistors; AM-LCD; dynamic response; amorphous silicon; feedthrough voltage; a-IGZO; timing; falling edge; overdrive

## Introduction

Next generation ultra-high definition (UHD) displays have resolutions of 4K×2K (3840×2160 pixels) or 8K×4K (7680×4320 pixels) and support frame rates of up to 120 Hz [1]. For 3D displays or motion blur reduction by image interpolation, frame rates of 240 Hz or higher are needed [2]. Improvements to display resolution and frame rate both correspond to shorter time margin available for each pixel to complete charging, thus placing stringent requirements on the dynamic response of thin-film transistor (TFT) backplane technology for active-matrix liquid crystal displays (AM-LCDs) and active-matrix organic light-emitting diodes (AM-OLEDs). The dynamic response of the hydrogenated amorphous silicon (a-Si:H) TFT pixel electrode has been studied extensively in literature. The feedthrough voltage ( $\Delta V_p$ ), which results from gate-source overlap capacitance ( $C_{GS}$ ) and channel charge redistribution, is the main source of image flickering in AM-LCD operation and a key metric in TFT dynamic response [3]. Takabatake *et al.* reported a robust analytical model for  $\Delta V_p$  that is very consistent with

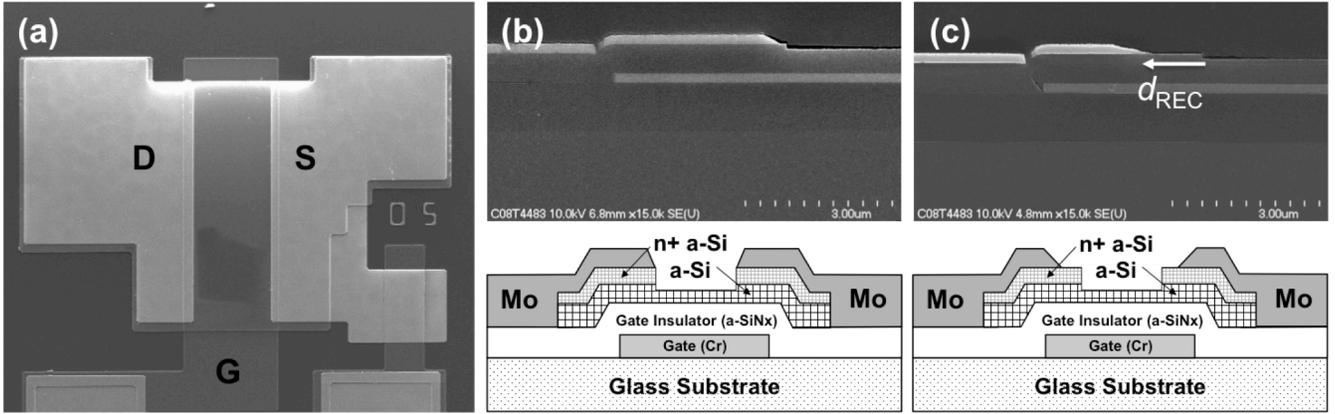
experimental values [4]. Kitazawa *et al.* investigated the impact of a-Si:H TFT device structural differences on  $\Delta V_p$  [5]. Aoki conducted a comprehensive study detailing an analytical model of a-Si:H TFT dynamic operation with the liquid-crystal cell capacitance included, and the model is verified by experimental data [6]. Lee *et al.* studied the dynamic response of a-Si:H TFT for AM-OLED pixel electrode, and reported in detail  $\Delta V_p$  and charging time ( $t_{CH}$ ) for various TFT structures and waveform parameters [7].

The amorphous In-Ga-Zn-O (a-IGZO) TFT, because of its superior field-effect mobility ( $\mu_{FE}$ ) on the order of 10 cm<sup>2</sup>/Vs and good electrical stability, has emerged as a leading candidate for next-generation active-matrix flat-panel display (AM-FPD) backplane technology [8]. Our group has previously described preliminary results on the dynamic response of a-IGZO TFT pixel electrodes in terms of its storage capacitance ( $C_{st}$ ) and TFT dimension dependences [9]. Initial data suggest that a-IGZO TFT showed very favorable dynamic characteristics when operated at a very high frequency. To date, however, there are still no comprehensive reports of a-IGZO TFT dynamic response published in peer-reviewed journal literature.

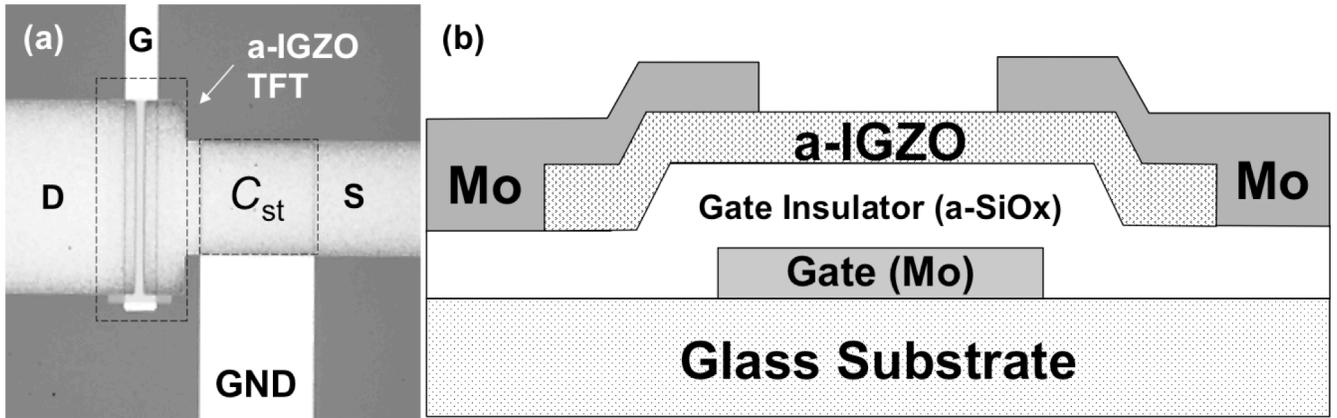
In this work, our objective is to evaluate and compare the dynamic response of a-Si:H and a-IGZO TFT in the context of pixel electrodes for UHD AM-FPDs. For all TFTs fabricated, charging characteristics are investigated for various gate waveform specifications. The equations governing  $\Delta V_p$  are thoroughly analyzed and the impact of the gate signal falling edge, gate voltage, and data voltage are studied in detail. The  $\Delta V_p$  as calculated from equation are used to verify the experimental values of  $\Delta V_p$  and its relationship with  $C_{st}$ . We also report the gate waveform overdrive operation of a-IGZO TFTs, which is expected to improve the dynamic response of a-IGZO TFT pixel electrodes with no drawbacks.

## Experiment

The fabrication of the BCE-type bottom-gate a-Si:H TFT follows the process described by Kuo *et al.* [10] and is briefly described here. The a-Si:H TFT has patterned chromium gate (200 nm) followed by two bilayers of amorphous silicon nitride (a-SiNx:H, 400 nm) and a-Si:H (170 nm), both deposited by PECVD. The interfacial a-SiNx:H and a-Si:H layers of the two bilayers are



**Figure 1.** (a) Top-view micrograph and (b) SEM image and cross-section diagram of the bottom-gate a-Si:H TFT used in this study. The SEM image and cross-section diagram of the a-Si:H TFT with the S/D-recess is shown in (c), where the recess length ( $d_{REC}$ ) is 1  $\mu\text{m}$ .



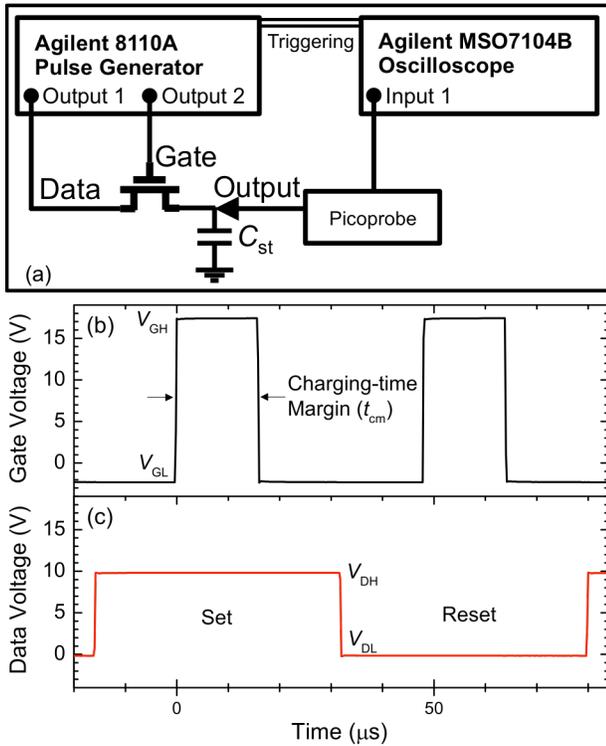
**Figure 2.** (a) Top-view micrograph and (b) cross-sectional diagrams and SEM images of the bottom-gate a-IGZO TFT used in this study.

deposited at lower deposition rates than the outer layers, and thus the channel-insulator interface region is of higher density and superior electronic property. A 70-nm layer of phosphorous-doped  $n^+$  a-Si:H is also deposited by PECVD to act as S/D contact regions. The active island is dry-etched using an  $\text{SF}_6:\text{Cl}_2:\text{O}_2:\text{He}$  gaseous mixture. The S/D electrodes are 200 nm of sputtered molybdenum (Mo) and are defined by wet etching with a phosphorous-nitric-acetic acid mixture. The resulting gate-S/D metal electrode overlap ( $OVLP$ ) is 3  $\mu\text{m}$ . During the S/D electrode definition, one set of TFTs (recessed TFTs) is intentionally over-etched for 160 s such that the Mo is also etched laterally, causing  $OVLP$  to be reduced to 2  $\mu\text{m}$  (recess length  $d_{REC} = 1 \mu\text{m}$ ). Lastly, we dry-etched ( $\text{HBr}:\text{Cl}_2$ ) the  $n^+$  a-Si:H and 70 nm of a-Si:H in the channel region. The a-Si:H TFT dimensions are width ( $W$ )/length ( $L$ ) = 57.5  $\mu\text{m}$ /7.5  $\mu\text{m}$ . The patterned photoresist remained on top of the Mo electrodes throughout the S/D definition steps and is removed at the end. We can approximate the gate-source capacitance in the area of overlap between the source and gate electrodes using the equation:

$$C_{GS} = W \times OVLP \times (C_{GI}^{-1} + C_{act}^{-1})^{-1}, \quad (1)$$

where  $C_{GI}$  is the gate insulator capacitance and  $C_{act}$  is the active layer (a-Si:H) capacitance. Using (1), we calculate  $C_{GS} = 0.021 \text{ pF}$  for normal TFTs and 0.014 pF for recessed S/D TFTs. The storage capacitor of  $C_{st} = 0.19 \text{ pF}$  is fabricated at the same time as the TFT using the gate insulator layer as dielectric (400 nm) and is connected in series to the TFT source terminal for the dynamic response test circuit. The a-Si:H TFT top-view micrograph and cross-section SEM images and diagrams illustrating the recess are shown in Fig. 1.

To fabricate the a-IGZO TFT, 100 nm of Mo is first deposited on a glass substrate (Corning Eagle or Asahi PD-200) using sputtering and then defined using dry etching. The gate insulator is 200 nm of PECVD amorphous silicon oxide (a-SiOx) deposited at 380  $^\circ\text{C}$ . The channel layer (50 nm) is then deposited by de-sputtering an a-IGZO target of composition  $\text{In}:\text{Ga}:\text{Zn}:\text{O} = 2:2:1:7$ . The a-IGZO active islands are defined using dilute oxalic acid (0.05 M) and then annealed in ambient air at 300  $^\circ\text{C}$  for 30 minutes on a hot plate. The gate vias are then opened using dry etching and subsequently 100 nm of Mo is sputtered during metallization. The S/D electrodes are defined using wet etching with 30%  $\text{H}_2\text{O}_2$ . The dimensions of the a-IGZO TFTs fabricated are  $W/L =$



**Figure 3.** (a) The schematic for the set-up used to evaluate the dynamic response of the one-TFT-one-capacitor test circuit. (b) The gate voltage applied is  $V_{GH} = 18$  V when charging/discharging and  $V_{GL} = -2$  V at all other times. The charging-time margin  $t_{cm}$  is the time available for the storage capacitor to completely charge/discharge. (c) The data voltage applied is  $V_{DH} = 10$  V for set and  $V_{DL} = 0$  V for reset. The set/reset duration is  $3 \times t_{cm}$ . The falling edge of the waveforms is 10 ns except where specified.

$74 \mu\text{m}/3 \mu\text{m}$  and  $OVL P = 5 \mu\text{m}$ . Using (1), we estimate  $C_{GS} = 0.06$  pF for the a-IGZO TFTs. After device processing, the TFTs undergo one final annealing step of  $300^\circ\text{C}$  for 30 minutes. For the dynamic response test circuit, a storage capacitor is fabricated in series with the a-IGZO TFT source terminal. To investigate the impact of storage capacitance, test circuits with  $C_{st} = 0.29$  pF,  $0.65$  pF, and  $1.15$  pF are evaluated in this study. The top-view micrograph and cross-section diagram of the a-IGZO TFT are shown in Fig. 2.

The set-up for evaluating the dynamic response of a-Si:H and a-IGZO TFTs is as follows: a two-channel HP 8110A pulse generator is connected to the drain and gate electrodes of the test circuit, where the drain is the data signal and the gate is the select signal. A low-input capacitance ( $0.02$  pF) and high-impedance (input leakage  $< 10$  fA) Picoprobe (HP18C-1-5-HV, GGB Industries) is used to measure the voltage of the storage capacitor  $C_{st}$  at the TFT source terminal. An Agilent MSO7104B oscilloscope is used to record the storage capacitor

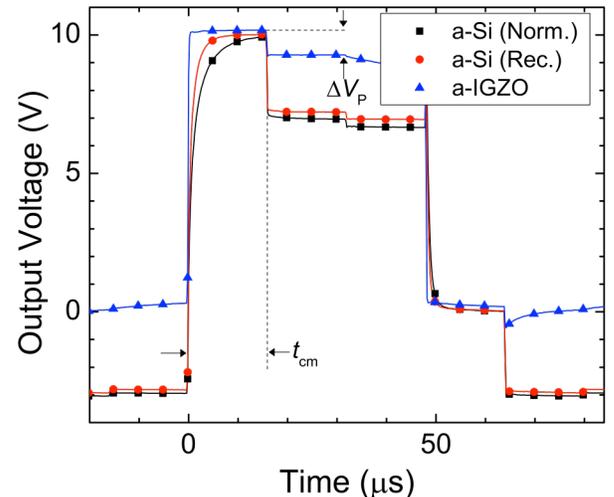
voltage measured by the Picoprobe with respect to time. Figure 3(a) shows the schematic for the set-up used in this study. The waveforms applied to the gate and data lines are shown in Figs. 3(b) and 3(c) respectively. For each frame, two gate pulses of  $V_{GH} = 18$  V are applied to the TFT gate electrode – one for set and another for reset. The low voltage of the gate waveform is  $V_{GL} = -2$  V. The gate pulse width, indicated in Fig. 3(b) as the charging-time margin ( $t_{cm}$ ), is the time available to charge/discharge  $C_{st}$  (for set/reset) in each pixel when the row lines are selected in AM-FPD operation. For a simple driving scheme without any charge sharing or pre-charging,  $t_{cm}$  is defined as [11]:

$$t_{cm} = \frac{1}{\text{Frame Rate} \times \text{Number of Row Lines}} \quad (2)$$

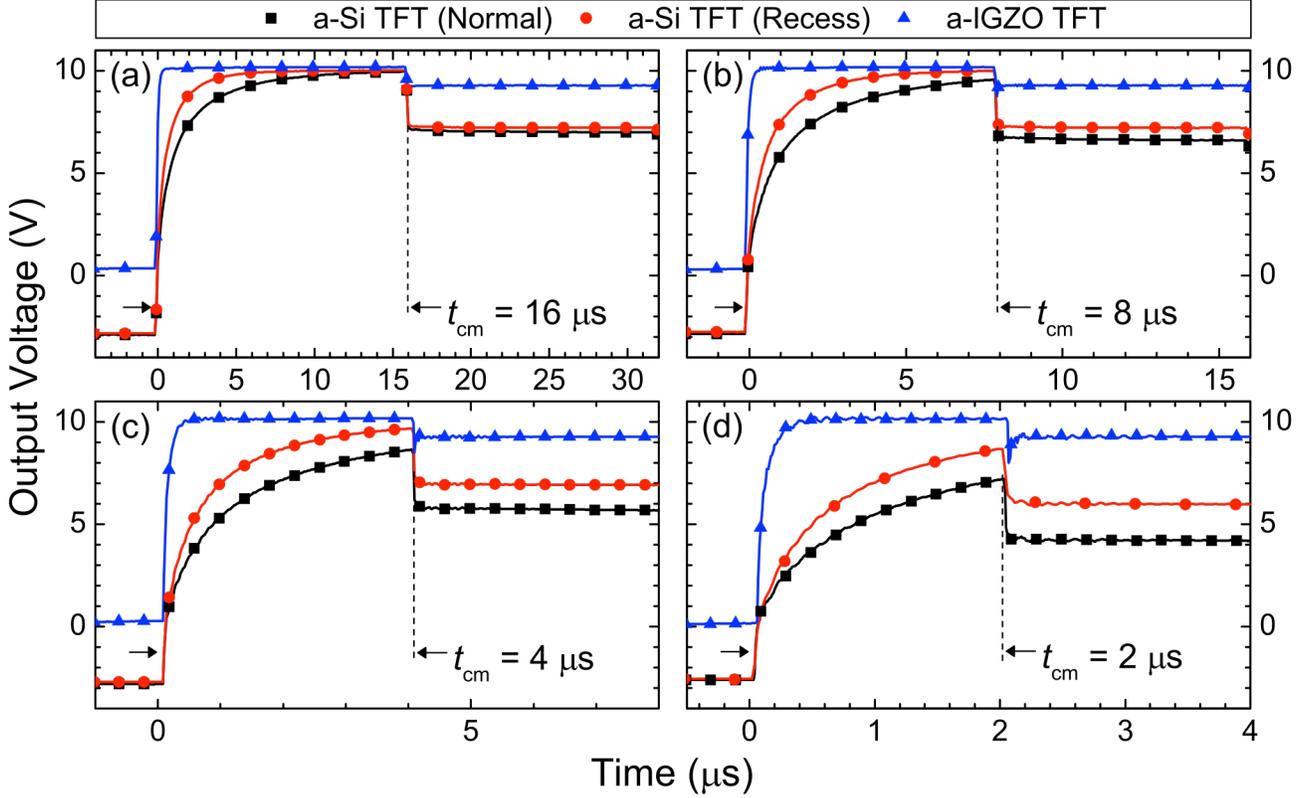
In this study, we are most interested in the charging-time margins corresponding to UHD AM-FPD resolutions and frame rates in [1]. Using (2), the  $t_{cm}$  are calculated based on these specifications and summarized in Table I. For

**Table 1.** The calculated charging-time margins based on AM-FPD resolution and frame rate specifications

Frame Rate	Resolution		
	Full HD (1920×1080)	4K UHD (3840×2160)	8K UHD (7680×4320)
60 Hz	15.4 $\mu\text{s}$ (16 $\mu\text{s}$ )	7.7 $\mu\text{s}$ (8 $\mu\text{s}$ )	3.9 $\mu\text{s}$ (4 $\mu\text{s}$ )
120 Hz	7.7 $\mu\text{s}$ (8 $\mu\text{s}$ )	3.9 $\mu\text{s}$ (4 $\mu\text{s}$ )	1.9 $\mu\text{s}$ (2 $\mu\text{s}$ )
240 Hz	3.9 $\mu\text{s}$ (4 $\mu\text{s}$ )	1.9 $\mu\text{s}$ (2 $\mu\text{s}$ )	0.96 $\mu\text{s}$ (1 $\mu\text{s}$ )
480 Hz	1.9 $\mu\text{s}$ (2 $\mu\text{s}$ )	0.96 $\mu\text{s}$ (1 $\mu\text{s}$ )	0.48 $\mu\text{s}$ (0.5 $\mu\text{s}$ )



**Figure 4.** The output voltage measured at the source terminal of the a-Si:H or a-IGZO TFTs with the data and gate waveform applied. The feedthrough voltage  $\Delta V_P$  is the output voltage drop at the end of  $t_{cm}$  after the gate voltage is flipped from  $V_{GH}$  to  $V_{GL}$ .



**Figure 5.** The output voltage at the source terminal of the a-Si:H and a-IGZO TFTs after applying the gate and data voltage waveforms based on (a)  $t_{cm} = 16 \mu s$ , (b)  $t_{cm} = 8 \mu s$ , (c)  $t_{cm} = 4 \mu s$ , (d)  $t_{cm} = 2 \mu s$ , corresponding to the AM-FPD specifications in Table I.  $C_{st}$  is 1.15 pF for a-IGZO TFTs and 0.19 pF for a-Si:H TFTs.

each frame, a single fixed pulse of data voltage  $V_{DH} = 10$  V is applied to the drain terminal for set, after which the data voltage is returned to its low level  $V_{DL} = 0$  V for reset. For the data voltage waveform, each set/reset period is defined to be  $3 \times t_{cm}$ . Each gate pulse arrives exactly  $1 \times t_{cm}$  after the data voltage is applied/removed. The rising and falling edge time ( $t_{FE}$ ) of the data and gate pulses are all 10 ns unless where specified. For falling edge values other than 10 ns, the corresponding rising edge is always 10% of that.

## Results and Discussion

### Charging Characteristics of a-Si:H and a-IGZO TFTs for Ultra-High Definition AM-FPDs

The output voltage ( $V_{out}$ ) at the source terminal of the a-Si:H or a-IGZO TFT as a function of time after applying the gate and data waveforms is shown in Fig. 4. In this figure, the gate and data waveforms are based on  $t_{cm} = 16 \mu s$ , which corresponds to Full HD 1080p resolution at 60 Hz – the current mainstream AM-LCD specification. In TFT pixel circuit dynamic response, one of the most important metrics is the storage capacitance charging behavior: incomplete charging directly causes the display gray-scale to deteriorate. In the figure, both a-Si:H TFTs

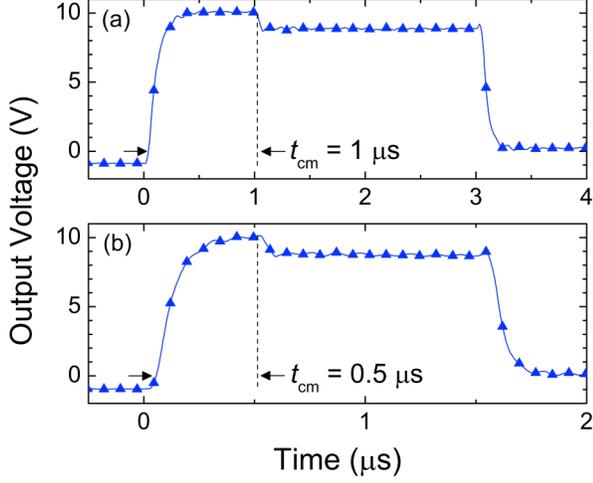
are able to charge completely to  $V_{DH} = 10$  V within 16  $\mu s$ , but the RC exponential charging curvature is clearly observable in the time-scale of the figure. In contrast,  $C_{st}$  charging by the a-IGZO TFT appears almost instantaneous. From the figure, we can extract the charging time constant ( $\tau$ ) at  $V_{out} = 6.3$  V (0.63  $V_{DH}$ ) for each device structure. The values of  $\tau$  are 1.35  $\mu s$ , 0.76  $\mu s$ , and 0.08  $\mu s$  for normal a-Si:H, recessed S/D a-Si:H, and a-IGZO TFT, respectively. The fact that the charging time constant of a-IGZO TFT is at least an order of magnitude lower than that of any a-Si:H TFT is mainly due to the much higher  $\mu_{FE}$  of a-IGZO. The charging behavior can be modeled by a simple RC model, in which the TFT drain current ( $I_D$ ) supplies the charges to the capacitor:

$$C_{st} \frac{dV_{out}}{dt} = I_D. \quad (3)$$

We can approximate  $I_D$  using the following simplified ideal MOSFET equation, which is appropriate for small drain-source voltages:

$$I_D = \mu_{FE} C_{GI} \frac{W}{L} (V_G - V_{out} - V_{th})(V_D - V_{out}). \quad (4)$$

The  $\mu_{FE}$  in (4) represents the TFT field-effect mobility. Combining (3) and (4), and solving for time, the elapsed



**Figure 6.** The output voltage at the source terminal of the a-IGZO TFTs after applying the gate and data voltage waveforms based on (a)  $t_{cm} = 1 \mu s$  and (b)  $t_{cm} = 0.5 \mu s$  corresponding to  $8K \times 4K$  resolution at 240 and 480 Hz. For this figure,  $C_{st} = 1.15 \text{ pF}$ .

time for charging  $C_{st}$  to a specific voltage  $V_S$  can be derived [7]:

$$t_{ch} = \frac{C_{st}L}{\mu_{FE}C_{GI}W} \frac{1}{(V_{GH} - V_{DH} - V_{th})} \ln \frac{(V_{GH} - V_{out} - V_{th})V_{DH}}{(V_{GH} - V_{th})(V_{DH} - V_{out})}. \quad (5)$$

Within the context of this study, we note from (5) that  $t_{ch}$  is directly proportional to  $C_{st}$  and inversely proportional to both  $W/L$  and  $\mu_{FE}$ . Considering that  $\mu_{FE}$  of a-IGZO is 1–2 orders of magnitude larger than a-Si:H, the fact that  $t_{ch}$  of a-IGZO TFT is much smaller than a-Si:H TFT is within our expectations, even though the a-IGZO TFT test circuit has a much larger  $C_{st}$ .

To highlight the advantage of a-IGZO TFT over a-Si:H TFT in terms of charging characteristics, we apply gate and data waveforms based on the charging-time margins in Table I, and show the resulting output voltages in Fig. 5 and Fig. 6. In Fig. 5(a), where  $t_{cm} = 16 \mu s$ , the a-Si:H TFTs are capable of fully charging  $C_{st}$  within the allotted time. As  $t_{cm}$  is reduced to  $8 \mu s$  and  $4 \mu s$  in Figs. 5(b) and 5(c), the a-Si:H TFTs begin to struggle to charge the storage capacitor. In Fig. 5(d), where  $t_{cm} = 2 \mu s$  represents the  $8K \times 4K$  UHD AM-FPD at 120 Hz, the a-Si:H TFTs can only charge  $C_{st}$  to 7.2 V (normal) and 8.7 V (recessed S/D). In real-world AM-LCD operation, gate and data bus-line RC delay may impose additional requirements for the charging-time margin [12], meaning that further degradations are expected for a-Si:H TFTs. In comparison, the simple BCE-type bottom-gate a-IGZO TFT is able to readily charge  $C_{st}$  to  $V_{DH} = 10 \text{ V}$  with ease for all four cases shown in Fig. 5. Charging behavior of the a-IGZO TFT pixel electrode is shown in Fig. 6 for (a)  $t_{cm} = 1 \mu s$  and (b)  $0.5 \mu s$ , corresponding to  $8K \times 4K$  resolution at 240 and 480 Hz, and the  $C_{st}$  is fully charged

to  $V_{DH}$  before the end of  $t_{cm}$ .

### Feedthrough Voltage of a-Si:H and a-IGZO TFTs

The feedthrough voltage ( $\Delta V_P$ ) indicated in Fig. 4 is the voltage drop at the TFT source terminal after the gate voltage flips from  $V_{GH}$  to  $V_{GL}$ . It was originally observed as clock feedthrough in CMOS switched-capacitor circuits, affecting its high-frequency accuracy [13]. In AM-FPD operation,  $\Delta V_P$  of the pixel electrode primarily manifests itself as image flickering [3]. The two primary contributions to  $\Delta V_P$  are capacitance feedthrough from  $C_{GS}$  to  $C_{st}$  and channel charge redistribution. Takabatake *et al.* developed a series of equations describing  $\Delta V_P$ , which we briefly summarize in the following discussion [4]. The capacitance feedthrough component of  $\Delta V_P$  can be calculated from:

$$\Delta V_{P,F} = \frac{C_{GS}}{C_{GS} + C_{st}} (V_{th} + V_{DH} - V_{GL}). \quad (6)$$

In (6), capacitance feedthrough is dependent on the ratio between  $C_{GS}$  and  $C_{st}$ . Overlap capacitance can be completely eliminated through the use of a self-aligned structure [14–17], but is difficult to avoid in the commonly used bottom-gate structure such as the ones in this study. Channel charge redistribution occurs when the TFT switches to its OFF-state and the accumulated channel charge ( $Q_{ch}$ ) has to be released. We can estimate  $Q_{ch}$  in the area of overlap ( $A$ ) between the gate electrode and the active layer with the equation:

$$Q_{ch} = C_{GI}A(V_{GH} - V_{th} - V_{DH}). \quad (7)$$

In our TFTs, we calculate the overlap area as  $A = W \times (L + 2OVLP)$ . When the gate signals falls abruptly from  $V_{GH}$  to  $V_{th} + V_{DH}$ , the TFT is turned off and any  $Q_{ch}$  in the channel is redistributed onto  $C_{st}$ :

$$\Delta V_{P,CR} = f \frac{Q_{ch}}{C_{st}} = f \frac{C_{GI}A(V_{GH} - V_{th} - V_{DH})}{C_{st}}, \quad (8)$$

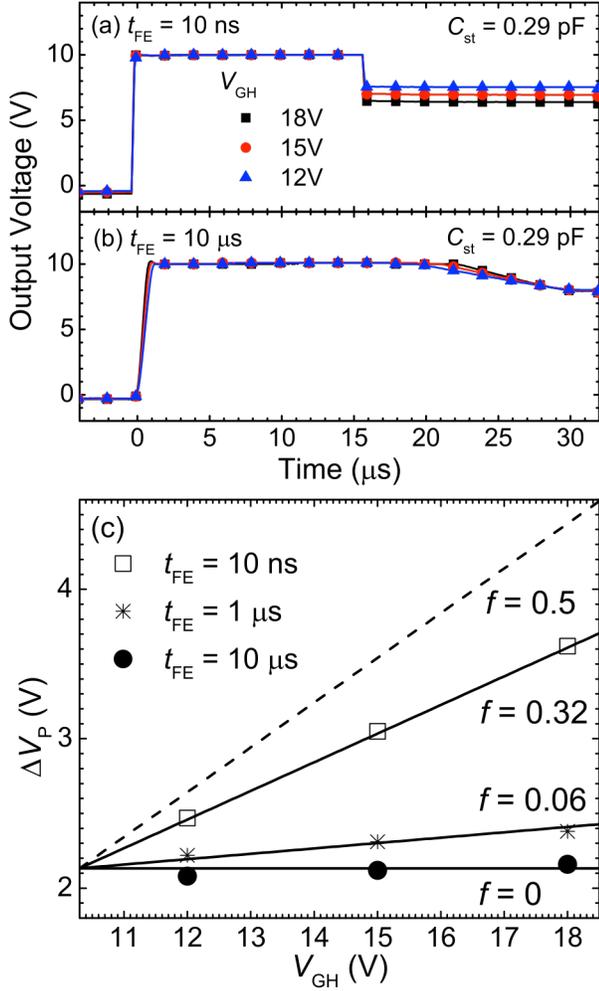
where  $f$  is a constant factor related to the gate falling edge. The total  $\Delta V_P$  is a sum of the (6) and (8) [4]:

$$\Delta V_P = \Delta V_{P,F} + \Delta V_{P,CR} = \frac{C_{GS}}{C_{GS} + C_{st}} (V_{th} + V_{DH} - V_{GL}) + f \frac{C_{GI}A(V_{GH} - V_{th} - V_{DH})}{C_{st}}. \quad (9)$$

The upper limit for  $f$  is exactly 0.5, for which the TFT is turned off so abruptly that no charges can be released through the drain terminal while  $V_G$  is reduced from  $V_{GH}$  to  $V_{th} + V_{DH}$ . In this upper limit, the gate voltage falling edge ( $t_{FE}$ ) satisfies the condition:

$$t_{FE} \ll \frac{L^2}{\mu_{FE} \Delta V_{P,CR}}. \quad (10)$$

The right-hand side of (10) is the channel transit time for accumulated charges. For  $t_{FE}$  below this upper limit,  $f$  decreases monotonically until it approaches the lower



**Figure 7.** The output voltage of the a-IGZO TFT test circuit for waveforms with  $V_{GH}$  varied from 18 V to 12 V for (a)  $t_{FE} = 10$  ns and (b)  $t_{FE} = 10$   $\mu$ s. The storage capacitance tested in this figure is 0.29 pF. In (c), the  $\Delta V_P$  extracted for  $t_{FE} = 10$  ns (empty squares), 1  $\mu$ s (solid circles), and 10  $\mu$ s (asterisks) are shown. The calculated  $\Delta V_P$  values are also shown in the figure for  $f = 0$  to 0.5.

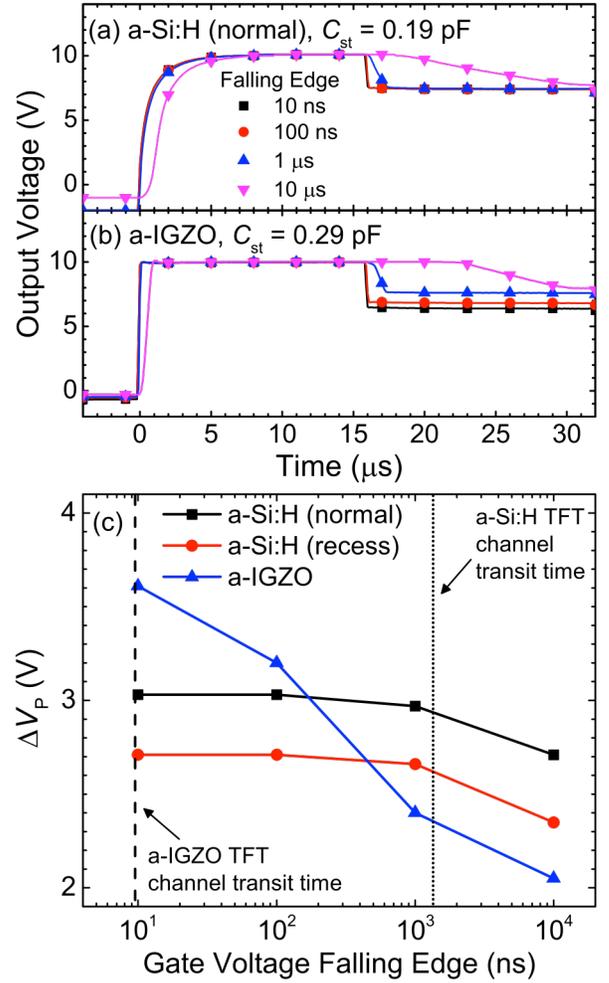
limit of  $f = 0$ . In this lower limit,  $t_{FE}$  is much slower than channel transit time of the charge carriers:

$$t_{FE} \gg \frac{L^2}{\mu_{FE} \Delta V_{P,CR}}. \quad (11)$$

In this case, most if not all of  $Q_{ch}$  can be released through the drain terminal while  $V_G$  is reduced from  $V_{GH}$  and  $V_{th} + V_{DH}$ . Contribution from (8) becomes negligible ( $f \approx 0$ ) and the total feedthrough voltage is simply:

$$\Delta V_P = \Delta V_{P,F} = \frac{C_{GS}}{C_{GS} + C_{st}} (V_{th} + V_{DH} - V_{GL}) \quad (12)$$

We note that according to (12),  $\Delta V_P$  does not depend on  $V_{GH}$  for slow  $t_{FE}$ . We can experimentally verify this by



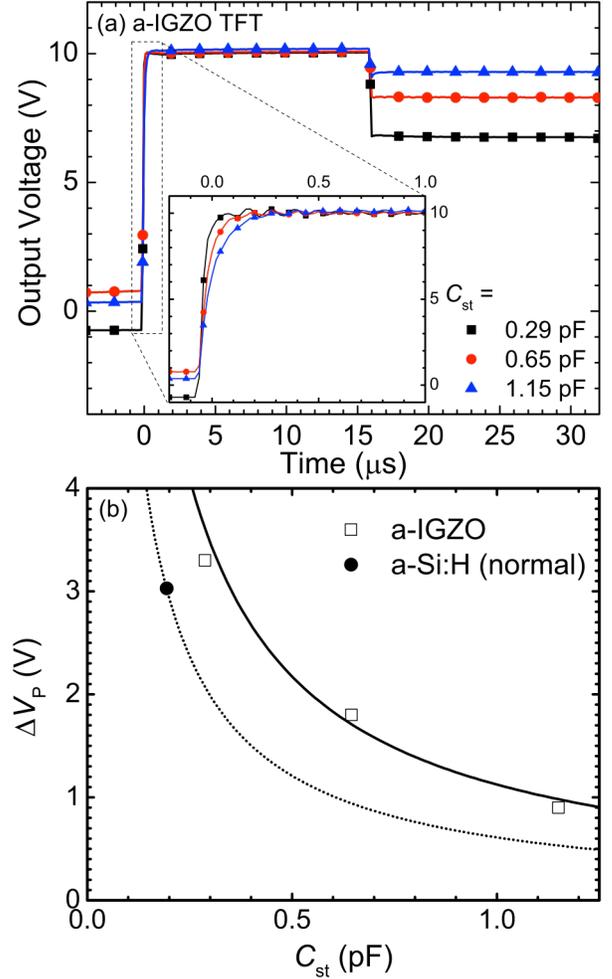
**Figure 8.** The output voltage of the a-IGZO and a-Si:H TFT test circuit for waveforms with  $t_{FE}$  varied from 10 ns to 10  $\mu$ s for (a) a-Si:H (normal) and (b) a-IGZO TFTs. The storage capacitance tested in this figure is 0.19 pF and 0.29 pF for the a-IGZO and a-Si:H TFTs, respectively. The  $\Delta V_P$  are extracted from (a) and (b) and shown in (c). The  $\Delta V_P$  for the recessed S/D a-Si:H TFT is also shown in (c). Using (10), the channel transit time is calculated and denoted (c) as dashed line and dotted line for a-IGZO and a-Si:H TFTs.

comparing the  $V_{GH}$  dependence of  $\Delta V_P$  for slow and fast  $t_{FE}$ . The output voltage of the a-IGZO TFT test circuit is shown in Fig. 7, where the falling edge of the gate pulse is (a)  $t_{FE} = 10$  ns and (b)  $t_{FE} = 10$   $\mu$ s. In Fig. 7(c),  $\Delta V_P$  corresponding to different  $V_{GH}$  are extracted for  $t_{FE} = 10$   $\mu$ s, 1  $\mu$ s, and 10 ns. Only  $V_{GH} \geq 10.3$  V ( $V_{th} + V_{DH}$ ) are shown in the figure, below which the TFT is in the off region and the equation has no meaning. We first calculate the  $\Delta V_P$  for various  $V_{GH}$  using (9) with  $f = 0.5$  and we find that the generated values are much larger than the experimental data for  $t_{FE} = 10$  ns. This means that the actual fast- $t_{FE}$  limit for a-IGZO TFTs is much smaller than

10 ns. Using (10), we calculate the channel transit time of the a-IGZO TFT to be 9.2 ns. This is consistent with what we observe in Fig. 7(c) in that (10) is not satisfied and  $f < 0.5$ . For  $t_{FE} = 10$  ns, we find that (9) with  $f = 0.32$  models the experimental data very well. In the same figure,  $\Delta V_p$  appears to be independent of  $V_{GH}$  for  $t_{FE} = 10$   $\mu$ s and can be well described by (12). This means that  $t_{FE} = 10$   $\mu$ s, which is three orders of magnitude larger than the channel transit time, can be considered as the slow- $t_{FE}$  limit and (10) is satisfied.

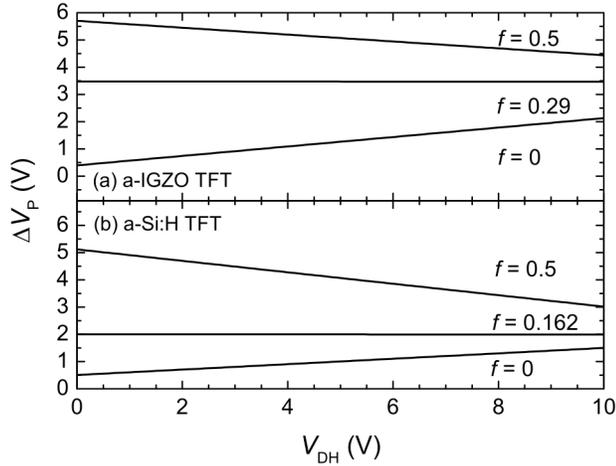
In Fig. 8, we compare the impact of  $t_{FE}$  on the  $\Delta V_p$  of (a) normal a-Si:H and (b) a-IGZO TFT by varying  $t_{FE}$  from 10 ns to 10  $\mu$ s. The extracted  $\Delta V_p$  at various  $t_{FE}$  are shown in Fig. 8(c) for normal a-Si:H, recessed S/D a-Si:H, and a-IGZO TFTs. For a change of three orders of magnitude in  $t_{FE}$ ,  $\Delta V_p$  decreases by only 0.3 V for the a-Si:H TFT. Actually,  $\Delta V_p$  appears to be almost unchanged from  $t_{FE} = 10$  ns to 1  $\mu$ s. In contrast,  $\Delta V_p$  decreases by 1.6 V for the same range of  $t_{FE}$  values. This significant difference is primarily due the fact that the  $\mu_{FE}$  of a-IGZO is more than an order of magnitude larger than that of a-Si:H, which would allow (10) to be fulfilled at a lower  $t_{FE}$ . We calculate the channel transit time to be 1.2  $\mu$ s for a-Si:H TFTs and it is shown in Fig. 8(c) together with that for a-IGZO TFTs. Our experimental observations are consistent with these two values in that for a-Si:H TFTs,  $\Delta V_p$  remains almost constant for  $t_{FE} < 1$   $\mu$ s. The  $\Delta V_p$  for the recessed S/D a-Si:H TFT is also shown, which is similar to the normal a-Si:H TFT curve shifted downward with the overall trend remaining the same. Considering that the only difference between normal and recessed TFTs is the reduction in  $C_{GS}$ , it is within our expectations that recessed S/D electrodes have no impact on the determination of fast- vs. slow- $t_{FE}$ . For a-IGZO TFTs,  $\Delta V_p$  is seen to be decreasing for all  $t_{FE}$  because no  $t_{FE}$  faster than 10 ns is tested in this study. An implication of Fig 8 is that for the a-IGZO TFT pixel electrode, because of the shorter channel transit time, it may be possible to reduce  $\Delta V_p$  by controlling for  $t_{FE}$ , while the same is difficult to realize for a-Si:H TFTs.

To study the impact of  $C_{st}$  on the dynamic response of a-IGZO TFT test circuits, the output voltage for circuits with three different storage capacitances are characterized and shown in Fig. 9(a). The  $t_{FE}$  for the waveforms applied are all 10 ns. From the figure, we observe that larger  $C_{st}$  corresponds to higher charging times and lower  $\Delta V_p$ , which is what we expect based on the previous analyses. The difference in terms of charging time is insignificant in this time-scale ( $t_{cm} = 16$   $\mu$ s) and only observable in the Fig. 9(a) inset. Of particular interest is the  $\Delta V_p$ , which we extract to be 3.3 V, 1.8 V, and 0.9 V for  $C_{st} = 0.29$  pF, 0.65 pF, and 1.15 pF, respectively, and shown in Fig. 9(b) as empty squares. The  $\Delta V_p$  for the normal a-Si:H TFT ( $C_{st} = 0.19$  pF) is extracted from Fig. 4 to be 2.71 V and is shown in the same figure as a solid circle. From (9), we calculate and show the relationship between  $C_{st}$  and  $\Delta V_p$



**Figure 9.** (a) The output voltage at the source terminal of a-IGZO TFT test circuits with different storage capacitances. The charging-time margin used for this figure is  $t_{cm} = 16$   $\mu$ s. (b) The  $\Delta V_p$  for a-IGZO TFTs with different  $C_{st}$  extracted from (a) is shown as empty squares. The  $\Delta V_p$  is calculated using (9) and shown in the figure as solid line ( $f = 0.32$ ) and dashed line ( $f = 0.5$ ). The normal a-Si:H TFT  $\Delta V_p$  is also shown in the figure as a solid circle, with the calculated value ( $f = 0.5$ ) represented as a dotted line.

for a-Si:H (dotted line) and a-IGZO TFTs (solid line) in Fig. 9(b). We observe that because of device structure and material properties, the a-IGZO TFT has greater  $\Delta V_p$  than the normal a-Si:H TFT for the same  $C_{st}$ . However, it should be pointed out that design of TFT pixel electrode does not have to assume identical  $C_{st}$  when considering a-Si:H vs. a-IGZO TFTs. The  $\Delta V_p$  of a-IGZO TFTs can easily be mitigated below that of a-Si:H TFTs by implementing a larger storage capacitor. Increasing  $C_{st}$ , as shown in Fig. 9(a), has negligible impact on charging behavior of the a-IGZO TFT pixel electrode. The limiting factor in this case would not be charging-time margin, but

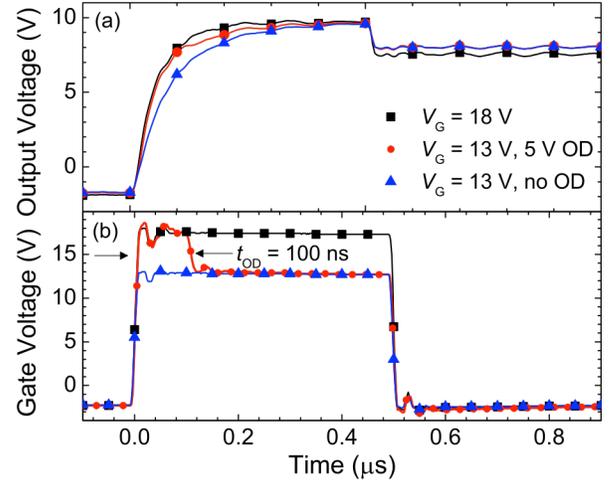


**Figure 10.** The pixel circuit feedthrough voltage vs.  $V_{DH}$  for (a) a-IGZO TFT ( $C_{st} = 0.29$  pF) and (b) a-Si:H TFT ( $C_{st} = 0.19$  pF). Various  $f$  values are shown for both TFTs

rather the aperture ratio of the AM-LCD pixel. This also bodes well for a-IGZO TFTs as the backplane technology of large-area AM-LCDs, which have larger liquid-crystal cells and thus greater cell capacitance.

For the recessed S/D a-Si:H TFT,  $\Delta V_P$  is extracted from Fig. 4 to be 2.71 V. Since the S/D-recess improves  $\Delta V_P$  without inducing any degradations in charging characteristics, it should be a useful technique in a-Si:H TFT fabrication. We note that the discrepancy between experimental and calculated values is much larger in this case, where 2.33 V is calculated from (9) assuming  $OVLP = 2$   $\mu\text{m}$ . Although the metal S/D electrodes are recessed by 1/3, the  $n^+$  a-Si:H S/D contact regions remain unmodified. This makes simple areal estimation of  $C_{GS}$  appropriate only for normal bottom-gate TFT structure without recess.

Now that the model described by (9) has been verified by experimental data for a-IGZO and a-Si:H TFTs, we can also use it to explore some other parameters that may potentially impact TFT pixel electrode operation in AM-FPDs. We note that (9) is dependent on  $V_{DH}$  for both high- or low- $t_{FE}$  limits because  $V_{DH}$  contributes to both capacitance feedthrough and charge redistribution. During AM-FPD operation, column drivers apply the various data voltage to the TFT drain terminal to program the pixel. Therefore, it is informative to explore the relationship between  $V_{DH}$  and  $\Delta V_P$ . We fix  $V_{GH} = 18$  V and  $C_{st} = 0.29$  pF for a-IGZO and 0.19 pF for a-Si:H TFTs. The  $\Delta V_P$  is calculated for  $V_{DH}$  from 0 V to 10 V and shown in Fig. 10 (a) for a-IGZO and (b) for a-Si:H TFTs. From the figure, we see that the dependence of  $\Delta V_P$  on  $V_{DH}$  actually changes with  $f$ , which correspond to different  $t_{FE}$ . Generally, for  $f = 0.5$ , which corresponds to the low  $t_{FE}$  limit,  $\Delta V_P$  is higher for high  $V_{DH}$ . In the high  $t_{FE}$  limit where  $f = 0$ ,  $\Delta V_P$  is higher for low  $V_{DH}$ . We see in both sub-figures that there exist a value of  $f$  for which  $\Delta V_P$



**Figure 11.** The overdrive operation of the a-IGZO TFT in the test circle is shown in (a). The waveforms for baseline, overdrive, full overdrive is shown in (b). Overdrive operation adds  $t_{OD} = 100$  ns of  $V_{OD} = 5$  V on top of the baseline  $V_{GH} = 13$  V at the beginning of  $t_{cm}$ . In full overdrive, the entire duration of  $t_{cm}$  is  $V_{GH} = 18$  V. For this experiment, test circuit with  $C_{st} = 0.65$  pF is evaluated.

appears to be independent of  $V_{DH}$ . This could potentially allow for a simple compensation scheme in which a constant DC offset is applied to the TFT pixel voltage for a fixed  $\Delta V_P$ . For a-IGZO TFT, this corresponds to  $f = 0.29$ , which is only slightly lower than  $f = 0.32$  of  $t_{FE} = 10$  ns, and could realistically be achieved with minor adjustments to  $t_{FE}$ . In a-Si:H TFT, this value is  $f = 0.162$ . However, considering that  $\Delta V_P$  barely changed even in the case of  $t_{FE} = 10$   $\mu\text{s}$ , we can conclude that such  $t_{FE}$  would be unrealistic in AM-FPD operation. Such versatility is another reason to consider a-IGZO TFTs superior to a-Si:H TFTs.

### a-IGZO TFT Pixel Electrode Overdrive Operation for Future Active-Matrix Flat-Panel Displays

Overdrive operation was initially proposed for operation of individual AM-LCD cells to improve the gray-level response for high-speed motion images [18–20]. The idea is that because there is a time delay in the gray-level transitions of a liquid crystal cell, the image signal can be pre-processed and an additional voltage (overdrive voltage  $V_{OD}$ ) can be added on top of the image signal to help the LC reach the desired transmittance faster. However, within published literature, the TFT has rarely been considered in the study of the overdrive method for AM-LCDs. In this work, we apply the voltage overdrive method to the gate signal of the a-IGZO TFT test circuit and the results are shown in Fig. 11 for  $C_{st} = 0.65$  pF. As shown in Fig. 11(b), three different gate waveforms are tested:  $V_{GH} = 18$  V (fully overdriven),  $V_{GH} = 13$  V + 5 V (overdrive time  $t_{OD} = 100$  ns), and  $V_{GH} = 13$  V (baseline).

Alternatively, we can also consider  $V_{GH} = 18$  V as the baseline,  $V_{GH} = 13$  V + 5 V ( $t_{OD} = 100$  ns) as partially underdriven, and  $V_{GH} = 13$  V as fully underdriven. From Fig. 11(a), we see that the overdrive method (solid circles) is a good balance of both improved charging time compared to  $V_{GH} = 13$  V and lower  $\Delta V_p$  than  $V_{GH} = 18$  V. In our previous work, we have shown that reducing the duration of high gate voltage ( $V_{GH}$ ) in pulsed waveforms of a-IGZO TFT dynamic operation improves the ac bias-temperature stress (BTS) stability [17]. The partially underdriven method proposed in this study is expected to help reduce ac BTS instability and still retain adequate charging characteristics. It should be noted that voltage overdrive may also be applicable to the data signal line, but is outside the scope of this study and should be investigated in future works.

### Conclusion

To evaluate the dynamic response of a-Si:H and a-IGZO TFTs, we have fabricated test circuits in which a TFT is connected to a storage capacitor at the source terminal. For the a-Si:H TFTs, in addition to the normal TFT configuration, we also fabricated the recessed S/D TFT where the S/D electrodes are intentionally over-etched to reduce the gate-S/D overlap. Waveforms corresponding to current- and next-generation AM-FPD specifications are tested. In our results, the recessed S/D a-Si:H TFTs have superior charging behavior and lower  $\Delta V_p$  when compared to normal a-Si:H TFTs, but both are still insufficient and cannot be used for 4K×2K or 8K×4K UHD AM-FPDs. Out of all three TFT structures tested, the a-IGZO TFT is shown to be fully capable of completely charging the storage capacitance within the charging-time margins for 8K×4K resolution at 240 and 480 Hz.

Analytical expressions describing the feedthrough voltage  $\Delta V_p$  are investigated in detail. In particular, the impact of the gate signal falling edge  $t_{FE}$  is thoroughly studied. We find that in the fast- $t_{FE}$  limit, channel charge redistribution and overlap capacitance feedthrough both contribute to  $\Delta V_p$ . For  $t_{FE}$  much larger than the channel transit time (slow- $t_{FE}$  limit) – approximately three orders of magnitude above the transit time – accumulated channel charges are almost completely released through the source electrode and do not contribute to  $\Delta V_p$ . The size of the storage capacitor is shown to have a strong impact on the  $\Delta V_p$  of a-IGZO TFT test circuits, but negligible influence on the charging behavior of  $C_{st}$ . Calculations show that for the same  $C_{st}$ ,  $\Delta V_p$  is larger for the a-IGZO TFT compared to the a-Si:H TFT. Increasing the size of  $C_{st}$  can reduce the  $\Delta V_p$ , and for a-IGZO TFTs this can be done without sacrificing charging behavior and only the aperture ratio would be affected.

Lastly, we have demonstrated overdrive operation of the a-IGZO TFT pixel electrode by increasing the gate voltage beyond the pre-defined  $V_{GH}$  for a short interval

within  $t_{em}$ . Our results show that overdrive operation allows for adequate charging behavior while  $\Delta V_p$  is decreased. With its versatility and superior performance, the a-IGZO TFT is a very promising and suitable candidate as the backplane technology for next-generation large-area UHD AM-FPDs.

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